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09/522,510	03/10/2000	Youfeng Wu	884.258US1	5136	
	7590 02/13/2003				
_	Lundberg Woessner	EXAMINER			
P O Box 2938 Minneapolis,		WOOD, WILLIAM H			
	٠		ART UNIT	PAPER NUMBER	
		2124			
			DATE MAILED: 02/13/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

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•••	_		Applicati	on No.	Applicant(s)	7	
		09/522,5	10	WU, YOUFENG			
	Offic	Action Summary	Examine	r	Art Unit		
			William H		2124		
Period fe	The MAII or Reply	LING DATE of this commu	nication appears on th	e cover sheet wit	th th correspondence address	ş	
THE - External afternal aftern	MAILING [ ensions of time or SIX (6) MONT e period for repl O period for rep ure to reply with reply received	O STATUTORY PERIOD IN COMMUNICATE OF THIS COMMUNICATE OF THIS COMMUNICATE OF THE PROVISION HS from the mailing date of this communicate of the communication of the set of extended period for reploy the Office later than three months adjustment. See 37 CFR 1.704(b).	IICATION. s of 37 CFR 1.136(a). In no exmunication. 30 days, a reply within the statatutory period will apply and w y will, by statute, cause the app	vent, however, may a re tutory minimum of thirty vill expire SIX (6) MON plication to become AB	eply be timely filed  (30) days will be considered timely.  THS from the mailing date of this commun  ANDONED (35 U.S.C. § 133).	lication.	
1)🛛	Respons	sive to communication(s) f	iled on <u>22 November</u>	<u> 2002</u> .			
2a) <u></u> ☐	This acti	on is <b>FINAL</b> .	2b) This action is	non-final.			
3)					ters, prosecution as to the me	erits is	
Disposit	closed in tion of Cla	accordance with the practims	ctice under <i>Ex parte</i> G	<i>≀uayle</i> , 1935 C.L	J. 11, 453 O.G. 213.		
4)🛛		1-28 is/are pending in the	• •				
	•	above claim(s) is/a	are withdrawn from co	onsideration.			
5)	Claim(s)	is/are allowed.					
·		1-28 is/are rejected.					
7)		is/are objected to			a.		
8) Applicat	ِ (Claim(s t <b>ion Paper</b>	are subject to restri s	ction and/or election r	requirement.			
9)	The specif	ication is objected to by th	ne Examiner.				
10)🛛	The drawir	ng(s) filed on <u>10 March 20</u>	<u>000</u> is/are: a) <u>□</u> accepto	ed or b) 🔀 objecte	ed to by the Examiner.		
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11)	The propo	sed drawing correction file	ed on is: a) 🔲 a	ipproved b)∏ di	sapproved by the Examiner.		
_		ed, corrected drawings are re		ffice action.			
•		r declaration is objected t	o by the Examiner.				
Priority	under 35 l	J.S.C. §§ 119 and 120					
13)	Acknowle	dgment is made of a clain	n for foreign priority u	nder 35 U.S.C. §	119(a)-(d) or (f).		
a)	)□ All b)[	☐ Some * c)☐ None of:					
	1. Certified copies of the priority documents have been received.						
	2. Certified copies of the priority documents have been received in Application No						
* ;		pies of the certified copies application from the Inter ached detailed Office action	national Bureau (PCT	Rule 17.2(a)).	received in this National Stag received.	е	
14) 🔲 .	Acknowled	gment is made of a claim	for domestic priority u	nder 35 U.S.C.	§ 119(e) (to a provisional appl	lication).	
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Attachme		_	, ,				
2) Noti	ce of Draftspe	ces Cited (PTO-892) erson's Patent Drawing Review ( osure Statement(s) (PTO-1449) i			Summary (PTO-413) Paper No(s) nformal Patent Application (PTO-152		

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#### **DETAILED ACTION**

Claims 1-28 have been examined.

#### Information Disclosure Statement

The Information Disclosure Statements filed on 10 March 2000 and 26 November
 2002 have been considered.

# **Drawings**

- 2. The drawings submitted were approved by the draft person.
- 3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show "predicate register" as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

## Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 5. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Hall, "Call Path Profiling" published in 1992.

In regard to claim 11, Hall disclosed the limitations:

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i) periodically sampling registers to obtain register values (page 299, section 5; indicates sampling profilers)

ii) storing an occurrence frequency of the register values in a data structure (page 299-300, section 5)

# Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Connors et al., "Compiler-Directed Dynamic Computation Reuse: Rational and Initial Results" in view of Rodiger et al. (USPN 5,960,198).

In regard to claim 1, Connors disclosed the limitations:

- i) computer-implemented method of profiling software (page 158, Abstract; page 164-165, section 4.2)
- ii) identifying a candidate reuse region (page 164, section 4)
- determining an input set for the candidate reuse region (page 162-163, section 3.1)

iv) profile set-values for the input set (page 162-165, section 3.1 and section 4.2)

Connors did not explicitly state *instrumenting* the code for profiling. Roediger demonstrated that it was known at the time of invention to use instrumenting profilers (column 3, line 63 to column 4, line 13). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' profiler with instrumentation in order to acquire the needed information as found in Roediger's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use a well known method of profiling to gather specifically required information. *Executing the instrumented software* is a step in profiling instrumented software (Roediger: column 4, liens 14-31).

In regard to claim 2, Connors and Roediger disclosed the limitations:

- i) identifying a candidate load instruction within the candidate reuse region (Connors: page 164-165, section 4.2)
- ii) instrumenting (as above in claim 1) the software to profile location-values for the candidate load instruction (Connors: page 164-165, section 4.2)

In regard to claim 5, the rejection of claim 1 is incorporated and further Connors and Roediger disclosed the limitation wherein instrumenting comprises inserting instructions to periodically sample set-values (Connors: page 162-163, section 3.1; page 164-165, section 4.2; Roediger: column 3, lines 63 to column 4, lines 13; sampling is also common to compilers).

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In regard to claim 8, Connors disclosed the limitation further comprising selecting the candidate reuse region as a computation reuse region (page 165, section 4.3).

In regard to claims 9 and 10, claim 9 is a machine readable medium claim corresponding to the method claim 1 and rejected under the same reason set forth under claim 1. The claim 10 is a machine readable claim corresponding to claim 5 and are rejected based upon the claim 1 rejection and the reasoning of claim 5.

7. Claims 3-4, 6, 11-12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Connors et al., "Compiler-Directed Dynamic Computation Reuse: Rational and Initial Results" in view of Roediger et al. (USPN 5,960,198) as applied to claim 1 and in further view of "Dictionary of Computing" herein referred to as Computing.

In regard to claim 3, Connors of claim 1 disclosed the limitations:

- wherein the input set comprises a plurality of input registers (page 162-163, section 3.1)
- input registers (page 162-163, section 3.1)

Connors did not explicitly state for each set-value, combining each of the input register values into a single value. This is merely a key into hashing. Computing demonstrated that it was known at the time of invention to use a key to access a table of information

(page 221; *hashing*). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' storage of reuse information with the ability to use a single value (key) to access such information as found in Computing's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to utilize a well-known technique of storing and accessing information quickly and easily.

In regard to claim 4, neither Connors nor Roediger disclosed the limitations wherein combining comprises folding each of the input register values to create folded values and concatenating the folded values. Computing demonstrated that it was known at the time of invention to utilize folding and hashing using a key value (page 196 and 221; folding and hashing). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors's system with folding and hashing as found in Computing's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use simple direct and quick methods to access information.

In regard to claim 6, Connors disclosed the limitations:

<sup>1)</sup> wherein the input-set comprises a plurality of input registers (page 162-163, section 3.1)

ii) each set-value comprises an input register value for each of the plurality of input registers (page 162-163, section 3.1)

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Connors did not explicitly state for each set-value, combining each of the input register values into a single value. Computing demonstrated that it was known at the time of invention to use a key to access a table of information (page 221). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' storage of reuse information with the ability to use a single value (key) to access such information as found in Computing's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to utilize a well-known technique of storing and accessing information quickly and easily. Connors' Computation Reuse Buffer is the data structure indexed into with the single value (page 162-163, section 3.1).

In regard to claim 11, Connors disclosed the limitation *storing an occurrence frequency* of the register values in a data structure (page 162-163, section 3.1). Connors did not explicitly state *periodically sampling registers to obtain register values*. Computing demonstrated that it was known at the time of invention to sample periodically (page 431, top right column). Roediger demonstrated it was known at the time of invention to have profilers that sampled (column 3, line 63 to column 4, line 13). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' profiling system with sampling abilities as found in Computing's and Roediger's teachings. This implementation would have been obvious because one of ordinary skill in the art would be motivated to make use of profiling techniques that allow quick production of useful information.

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In regard to claim 12, the rejection of claim 11 immediately above is incorporated and further Computing and Connors disclosed the limitation wherein periodically sampling comprises sampling a plurality of registers to obtain a set-value every S occurrences of a candidate reuse region, where S is a sampling period. Computing demonstrated sampling every S occurrences, a regular basis (page 431, top right column). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' system of region reuse dependent on memory instructions with sampling on a regular basis as found in Computing's teachings. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use a common method and therefore well understood method of gathering information for use in optimizing a computer system. Connors is shown to be profiling set-values (page 162-163, section 3.1)

In regard to claim 14, the rejection of claim 12 is incorporated and further Connors disclosed the limitation *incrementing a profile indicator at the record* (Connors: alters the record accordingly or else would be useless). Connors did not explicitly state *storing comprises accessing a record in the data structure as a function of the set-value*. This is merely a key into hashing. Computing demonstrated that it was known at the time of invention to use a key to access a table of information (page 221). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' storage of reuse information with the ability to use a single value (key) to

access such information as found in Computing's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to utilize a well-known technique of storing and accessing information quickly and easily.

Connors' Computation Reuse Buffer is the data structure indexed into with the single value (page 162-163, section 3.1)

In regard to claim 15, the rejection of claim 12 is incorporated and further Connors, Roediger and Computing disclosed the limitations:

- wherein periodically sampling further comprises sampling set-values in the plurality of registers at the beginning of a candidate reuse region (Connors: page 165-166, sections 4.3 and 4.4; Connors describes determining the entry points into the reuse region and needing to profile them)
- ii) the plurality of registers being input registers to the candidate reuse region (Connors: page 162, first paragraph in section 3.1)
- 8. Claims 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Connors et al., "Compiler-Directed Dynamic Computation Reuse: Rational and Initial Results" in view of Roediger et al. (USPN 5,960,198) as applied to claim 5 and in further view of Calder et al. "Value Profiling and Optimization".

In regard to claim 7, the rejection of claim 5 is incorporated, however Connors and Roediger did not explicitly state the limitation wherein instrumenting further comprises

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inserting instructions to profile the top N occurring set-values, where N is chosen as a function of an expected number of reuse instances. Calder demonstrated that it was known at the time of invention to profile the top N occurring values (page 1-2, Introduction). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors and Roediger's reuse profiling with profiling the top N occurring values as found in Calder's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use Value Profiling to its fullest as suggested by Connors' use of Value Profiling himself. Official Notice is taken that it was known at the time of invention to base a number of profilings on the expected number of instances. It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors, Roediger and Calder with the ability to capture N values if that number of reuse instances were expected to occur. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide as accurate as possible information during profiling, which would include if possible profiling N values if N were expected.

8. Claims 16, 17 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Connors et al., "Compiler-Directed Dynamic Computation Reuse: Rational and Initial Results" in view of Roediger et al. (USPN 5,960,198) in further view of Calder et al. "Value Profiling and Optimization" in view of "Dictionary of Computing" herein referred to as Computing.

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In regard to claim 16, Connors disclosed the limitations:

i) identifying a candidate load instruction (page 164-165, section 4.2, reusability of memory operations)

ii) executing the software (page 164-166, section 4)

Connors did not explicitly state instrumenting the software to sample a location-value every S occurrences of the candidate load instruction. Roediger demonstrated that it was known at the time of invention to use instrumenting profilers (column 3, line 63 to column 4, line 13). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' profiler with instrumentation in order to acquire the needed information as found in Roediger's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use a well known method of profiling to gather specifically required information. Calder demonstrated that it was known at the time of invention to profile for location-values in Value Profiling (page 16-23, section 6, especially page 16; page 5-11, section 3). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' system of region reuse dependent on memory instructions (a load being one of them) with Calder's Value Profiling mechanisms. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use Value Profiling to its fullest as suggested by Connors' use of Value Profiling himself. Computing demonstrated sampling every S occurrences, a regular basis (page 431). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' system of region reuse dependent on memory instructions with

sampling on a regular basis as found in Computing's teachings. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use a common method and therefore well understood method of gathering information for use in optimizing a computer system.

In regard to claim 17, the rejection of claim 16 is incorporated and further Calder disclosed the limitations:

- i) inserting instructions in the software to count the number of times each location-value is sampled (page 20, second full paragraph)
- ii) inserting instructions in the software to keep track of top location-values (page 5-11, section 3)

In regard to claim 20, the rejection of claim 17 is incorporated and further Calder disclosed the limitation wherein inserting instructions to keep track to top location-values includes inserting sampling instructions configured to profile the top N occurrences of location-values, where N is an integer (page 5-11, section 3).

In regard to claims 21 and 22, claim 21 is a machine readable medium claim corresponding to the method claim 16 and rejected under the same reason set forth under claim 16. The claim 22 is a machine readable claim corresponding to claim 17 and are rejected based upon the claim 16 rejection and the reasoning of claim 17.

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9. Claims 23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Connors et al., "Compiler-Directed Dynamic Computation Reuse: Rational and Initial Results" in view of Calder et al. "Value Profiling and Optimization".

In regard to claim 23, Connors disclosed the limitations concerning profiling set-values for selecting a canidate reuse region to be used based on probability (page 164-165, section 4.2; page 158-159, Introduction), however Connors did not explicitly state profiling top set-values to produce a probability the reuse region should be selected. Calder demonstrated that it was known at the time of invention to utilize top values (Calder: page 5-11, section 3). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' set-values of reuse regions with top values as found in Calder's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to fully implement the functionality of value profiling, which itself was suggested by Connors page 164.

In regard to claim 27, claim 27 is a machine readable medium claim corresponding to the method claim 23 and rejected under the same reason set forth under claim 23.

10. Claims 24-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Connors et al., "Compiler-Directed Dynamic Computation Reuse: Rational and Initial Results" in view of Calder et al. "Value Profiling and Optimization" as applied to

claim 23 and in further view of "Dictionary of Computing" herein referred to as Computing.

In regard to claim 24, Connors did not explicitly state *for each set-value, combining each of the input register values into a single value*. Computing demonstrated that it was known at the time of invention to use a key to access a table of information (page 221). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' storage of reuse information with the ability to use a single value (key) to access such information as found in Computing's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to utilize a well-known technique of storing and accessing information quickly and easily. Connors' Computation Reuse Buffer is the data structure indexed into with the single value (page 162-163, section 3.1).

In regard to claim 25, Connors did not explicitly state wherein accessing a data structure comprises accessing a data structure at least as large as a number of expected reuse instances. Official Notice is taken that it was known at the time of invention to create a structure large enough to hold all the expected values needed. It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors' Computation Reuse Buffer as being as large as necessary for all expected reuse regions. This implementation would have been obvious because one of ordinary skill in

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the art would be motivated to improve as much of the code as possible for better optimization.

In regard to claim 26, Connors disclosed the limitations wherein selecting comprises marking as reuse regions those candidate reuse regions having a finite number of top set-values that have probability of occurrence greater than a threshold (page 159, left column, first full paragraph; clearly some threshold must be used to gauge the effectiveness of the profiling, which produced some heuristics).

In regard to claims 28, claim 28 is a machine readable medium claim corresponding to the method claim 24 and rejected under the same reason set forth under claim 24.

11. Claims 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Connors et al., "Compiler-Directed Dynamic Computation Reuse: Rational and Initial Results" in view of Roediger et al. (USPN 5,960,198) and in further view of "Dictionary of Computing" herein referred to as Computing as applied to claim 12 and in further view of Chang (USPN 5,933,628).

In regard to claim 13, the rejection of claim 12 is incorporated, however Connors, Roediger and Computing did not explicitly state the limitations:

i) identifying a group of control equivalent candidate region entries and candidate load instructions

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ii) inserting instructions prior to the group, wherein the instructions set a predicate register every S occurrences

iii) inserting profiling instructions at each of the control equivalent candidate region entries and candidate load instructions, wherein the profiling instructions are predicated on the predicate register

Chang demonstrated that it was known at the time of invention to use predicate registers for decision control as in item iii) (Chang: column 5, line 52 to column 6, line 18). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors, Roediger and Computing's sampling and profiling of reuse regions system with predicate registers utilized by code as found in Chang's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to reduce the amount of branches in the code and thus speed up and lineate the whole operation. Official Notice is taken that it was known at the time of invention to instrument code as little as possible and hence use a small section of instrumentation code for multiple regions of the to be observed code, where possible as in item i) and ii). Thus, It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors, Roediger and Computing's sampling and profiling of reuse regions system with functionality to insert small amounts of instrumentation code which could observe several regions of the observable code. This implementation would have been obvious because one of ordinary skill in the art would be motivated to reduce the amount of damaging additional instrumentation code, and thus improve the efficiency of the profiling operation by allowing the overall code to

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behave as closely as possible to the original uninstrumented code. S occurrences is met in the same way as in claim 12 (Computing: page 431, top right column).

14. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Connors et al., "Compiler-Directed Dynamic Computation Reuse: Rational and Initial Results" in view of Roediger et al. (USPN 5,960,198) and in further view of "Dictionary of Computing" herein referred to as Computing in view of Calder et al. "Value Profiling and Optimization" as applied to claim 16 and in further view of Chang (USPN 5,933,628).

In regard to claim 18, the rejection of claim 16 is incorporated, however Connors, Roediger, Calder and Computing did not explicitly state the limitations:

- i) identifying a group of control equivalent candidate region entries and candidate load instructions
- ii) inserting instructions prior to the group, wherein the instructions set a predicate register every S occurrences
- iii) inserting profiling instructions at each of the control equivalent candidate region entries and candidate load instructions, wherein the profiling instructions are predicated on the predicate register

Chang demonstrated that it was known at the time of invention to use predicate registers for decision control (Chang: column 5, line 52 to column 6, line 18). It would have been obvious to one of ordinary skill in the art at the time of invention to implement

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Connors, Roediger, Calder and Computing's sampling and profiling of reuse regions system with predicate registers utilized by code as found in Chang's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to reduce the amount of branches in the code and thus speed up and lineate the whole operation. Official Notice is taken that it was known at the time of invention to instrument code as little as possible and hence use a small section of instrumentation code for multiple regions of the to be observed code, where possible as in item i) and ii). Thus, It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors, Roediger, Calder and Computing's sampling and profiling of reuse regions system with functionality to insert small amounts of instrumentation code which could observe several regions of the observable code. This implementation would have been obvious because one of ordinary skill in the art would be motivated to reduce the amount of damaging additional instrumentation code, and thus improve the efficiency of the profiling operation by allowing the overall code to behave as closely as possible to the original uninstrumented code. S occurrences is met in the same way as in claim 12 (Computing: page 431, top right column).

In regard to claim 19, the rejection of claim 17 is incorporated and further Calder disclosed the limitations:

i) wherein the candidate region includes a plurality of candidate load instructions (page 164-165, section 4.2; memory operations include load instructions)

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Calder did not explicitly state each of the plurality of load instructions being predicted on a common predicate register. Chang demonstrated that it was known at the time of invention to use predicate registers for decision control (Chang: column 5, line 52 to column 6, line 18). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Connors, Roediger, Calder and Computing's sampling and profiling of reuse regions system with predicate registers utilized by code as found in Chang's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to reduce the amount of branches in the code and thus speed up and lineate the whole operation.

### Conclusion

- 15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows.
  - a) Wu et al., "Better Exploration of Region-Level Value Locality with Integrated Computation Reuse and Value Prediction", taught a system of region reuse very similar to claimed invention. The publication date is after the claimed invention's filing date, but the authors are differing.
  - b) Watterson et al., "Goal-Directed Value Profiling", taught using value profiling with excellent examples and use of regions of code. Publication date is after the claimed invention's filing date.

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## Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (703)305-3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood February 3, 2003

KAKALI CHAKI

SUPERVISORY PATENT EXAMINATE
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